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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,009	RAMAKRISHNAN, SIVA	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

Claims 1-29 remain pending and are ready for examination.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The disclosure is objected to because of the following informalities:

- Paragraph 0011: The phrase 'mainmemory' appears.
- Paragraph 0012: The phrase 'performance impactsed by of compression' appears.
- Paragraph 0013: The phrase 'prioritization scheme for alleviating performance impacts association of with' appears.
- Paragraph 0020: The word 'The' appears at the end of the paragraph.
- Paragraph 0021: The paragraph begins with the phrase 'Subsequently, After the pointer is obtained,. Consequently the compressed ...' Correction is required with respect to the phrase and punctuation.
- Paragraph 0021: The phrase '... uncompressed form Before buffer ...' appears.

Appropriate correction is required.

Claim Objections

Claims 5, 21, and 26 are objected to because of the following informalities:

- Claim **5**, line 21, does not have any ending punctuation.
- Claim **21**, line 15, needs a space between the number '18' and the word 'wherein'.
- Claim **26**, line 25, needs a space between the phrase 'CMPTand.'

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 9-10, 15, 20, 22, 24, 26, and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim **5** recites the limitation "the entry" in line 18. There is insufficient antecedent basis for this limitation in the claim. Additionally in line 18, an entry is being evicted from the compression cache. The method used to evict the data from the compression cache, (i.e. LRU, FIFO, LIFO) is not instantly claimed. Additionally in line 21, the phrase, 'the data being compressed' appears. This is unclear, as there is no data that is being compressed. The Examiner is interpreting the applicant's to have meant that the actual address is of the data that is already compressed in compressed memory.

Claim **9** recites the limitation, 'memory address for which the data is compressed.' This is unclear. The Examiner is interpreting the applicant's to have meant, 'memory addresses for the plurality of compressed data.'

Claim **10** recites the limitation "the entry" in line 15. There is insufficient antecedent basis for this limitation in the claim. Additionally in line 15, an entry is being evicted from the compression cache. The method used to evict the data from the compression cache, (i.e. LRU, FIFO, LIFO) is not instantly claimed. Additionally in line 18, the phrase, 'of a data being compressed' appears. This is unclear, as there is no

data that is being compressed. The Examiner is interpreting the applicant's to have meant that the actual address is of the data that is already compressed in compressed memory.

Claim **15** recites the limitation "the compression cache" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim **20** recites the limitation "the apparatus" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim **22** recites the limitation "the entry" in line 22. There is insufficient antecedent basis for this limitation in the claim. Additionally in line 22, an entry is being evicted from the compression cache. The method used to evict the data from the compression cache, (i.e. LRU, FIFO, LIFO) is not instantly claimed. Additionally in lines 1-2, the phrase, 'of a data being compressed' appears. This is unclear, as there is no data that is being compressed. The Examiner is interpreting the applicant's to have meant that the actual address is of the data that is already compressed in compressed memory.

Claim **24** recites the limitation "the apparatus" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim **26** recites the limitation "the entry" in line 20. There is insufficient antecedent basis for this limitation in the claim. Additionally in line 20, an entry is being evicted from the compression cache. The method used to evict the data from the compression cache, (i.e. LRU, FIFO, LIFO) is not instantly claimed. Additionally in line 23, the phrase, 'of a data being compressed' appears. This is unclear, as there is no

data that is being compressed. The Examiner is interpreting the applicant's to have meant that the actual address is of the data that is already compressed in compressed memory.

Claim **28** recites the limitation "the apparatus " in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 9, and 14-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Benveniste et al (U.S. 6,353,871) herein after referred to as Benveniste. The instant claims are being rejected in light of the 35 U.S.C. 112 2nd paragraph rejections supra.

As per independent claim **1**, Benveniste teach,

- a compression cache to store a plurality of uncompressed data; (Column1 lines 52-52). *The Examiner is interpreting the buffers of Benveniste which store the uncompressed data to be the caches as instantly claimed.*
- a compressed memory to store a plurality of compressed data; and (Column 1 lines 44-47).
- a compressed memory pointer table (CMPT) to store a plurality of pointers (Column1 line 54 to Column 2 line 11). *The Examiner is interpreting the*

directory structure of Benveniste to be the pointer table that stores a plurality of pointers pointing to the data as instantly claimed. Each directory entry in the directory structure maintains an address or pointer to the respective data. Accordingly, the directory structure of Benveniste anticipates the pointer table as instantly claimed.

As per dependent claim **2**, Benveniste teach, wherein the compression cache is a sectored cache (Item 266 of Figure 2). *The Examiner notes that as discussed supra, the buffers of Benveniste anticipate the compression cache as instantly claimed. As shown in Figure 2, these buffers are individual and thus sectored. Accordingly Benveniste anticipates the compression cache as a sectored cache with the buffers.*

As per dependent claim **3**, Benveniste teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus (Column1 line 54 to Column 2 line 11). *The Examiner notes that the individual directory entries anticipate the tags.*

As per dependent claim **4**, Benveniste teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 1 line 54-60).

As per dependent claim **9**, Benveniste teach, wherein the CMPT stores the plurality of pointers to the plurality of compressed data sequentially based on memory address for which the data is compressed (Column 5 lines 49-62).

As per independent claim **14**, Benveniste teach,

- receiving a memory address for the memory operation; (Column 3 line 13)

- storing a plurality of compressed data in a main memory; and (Column 3 lines 24-26)
- performing a tag match between the memory address and a first cache storing a plurality of tags for a compressed memory in the main memory (Column 3 lines 15-20).

As per dependent claim **15**, Benveniste teach, accessing a plurality uncompressed data access from the compression cache is performed if the tag match resulted in a hit (Column 3 lines 20-25).

As per dependent claim **16**, Benveniste teach, locating a pointer and subsequently finding a compressed memory location based at least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss (Column 3 lines 10-30).

As per dependent claim **17**, Benveniste teach, compressing the data and storing it in a compressed memory location for the memory operation for a write miss (Column 3 lines 10-30).

As per independent claim **18**, Benveniste teach,

- a processor; and (Column 1 lines 38-39 and Figure 1 item 102) *The Examiner notes that a CPU as taught by Benveniste is a processor.*
- a main memory, coupled to the processor, with a (Figure 1 item 108).
- a compression cache to store a plurality of uncompressed data; (Column1 lines 52-52). *The Examiner is interpreting the buffers of Benveniste which store the uncompressed data to be the caches as instantly claimed.*

- a compressed memory to store a plurality of compressed data; and (Column 1 lines 44-47).
- a compressed memory pointer table (CMPT) to store a plurality of pointers (Column1 line 54 to Column 2 line 11). *The Examiner is interpreting the directory structure of Benveniste to be the pointer table that stores a plurality of pointers pointing to the data as instantly claimed. Each directory entry in the directory structure maintains an address or pointer to the respective data. Accordingly, the directory structure of Benveniste anticipates the pointer table as instantly claimed.*

As per dependent claim **19**, Benveniste teach, wherein the compression cache is a sectored cache (Item 266 of Figure 2). *The Examiner notes that as discussed supra, the buffers of Benveniste anticipate the compression cache as instantly claimed. As shown in Figure 2, these buffers are individual and thus sectored. Accordingly Benveniste anticipates the compression cache as a sectored cache with the buffers.*

As per dependent claim **20**, Benveniste teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus (Column1 line 54 to Column 2 line 11). *The Examiner notes that the individual directory entries anticipate the tags.*

As per dependent claim **21**, Benveniste teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 1 line 54-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-7, 10-12, 22-24, and 26-29 are rejected under 35 U.S.C. 103(a) as being obvious over Benvensite in view of Van Doren et al (U.S. 6,202,126) herein after referred to as Van Doren. The instant claims are being rejected in light of the 35 U.S.C. 112 2nd paragraph rejections supra.

As per dependent claim **5**, Benveniste teach, a CMPT offset calculator to provide an offset relative to the start of the CMPT based on an actual address of the data being compressed (Column 6 lines 20-34).

Benveniste does not teach, a victim buffer to store at least one the entry that has been evicted from the compression cache.

Van Doren teach, a victim buffer to store at least one the entry that has been evicted from the compression cache (Column 1 lines 10-12).

Benveniste and Van Doren are analogous art because they are from the same field of endeavor, namely cache memories.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Van Doren before him/her, to integrate the victim buffers of Van Doren into the system of Benveniste so displaced data from the cache has temporary storage.

The motivation for doing so would be that, "each CPU may also include victim buffers for temporarily storing data which is displaced from its cache (Column 1 lines 10-12 of Van Doren)."

Therefore, it would have been obvious to combine Benveniste with Van Doren to obtain the invention as specified in claims 5-7, 10-12, 22-24, and 26-29.

As per dependent claim **6**, Benveniste teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 2). *The Examiner notes that item 260 of Figure 2 is shown as a part of the whole system. Accordingly, item 260 is part of a chipset.*

As per dependent claim **7**, Benveniste teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset (Figure 3 item 260).

As per independent claim **10**, Benveniste teach,

- a first cache to store a plurality of tags for a compression cache; (Figure 3 item 320)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and (Column 6 lines 20-34).
- a second cache to store a plurality of pointers for the CMPT (Figure 3 item 330).

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache (Column 1 lines 10-12).

As per dependent claim **11**, Benveniste teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 2). *The Examiner notes that item 260 of Figure 2 is shown as a part of the whole system. Accordingly, item 260 is part of a chipset.*

As per dependent claim **12**, Benveniste teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset (Figure 3 item 260).

As per independent claim **22**, Benveniste teach,

- a processor; and (Column 1 lines 38-39 and Figure 1 item 102) *The Examiner notes that a CPU as taught by Benveniste is a processor.*
- a memory interface, coupled to the processor, with a: (Figure 1 item 108).
- a first cache to store a plurality of tags for a compression cache; (Figure 3 item 320)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; (Column 6 lines 20-34).
- and a second cache to store a plurality of pointers for the CMPT. (Figure 3 item 330).

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache; (Column 1 lines 10-12).

As per dependent claim **23**, Benveniste teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 2). *The Examiner notes that item*

260 of Figure 2 is shown as a part of the whole system. Accordingly, item 260 is part of a chipset.

As per dependent claim **24**, Benveniste teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset (Figure 3 item 260).

As per independent claim **26**, Benveniste teach,

- a processor, coupled to a memory bridge, the memory bridge to comprise; (Column 1 lines 38-39 and Figure 1 item 102) *The Examiner notes that a CPU as taught by Benveniste is a processor.*
- a first cache to store a plurality of tags for a compression cache; (Figure 3 item 320)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and (Column 6 lines 20-34).
- a second cache to store a plurality of pointers for the CMPT and (Figure 3 item 330).
- a main memory, coupled to the memory bridge, to comprise a (Figure 1 item 108).
- compression cache to store a plurality of uncompressed data; (Column1 lines 52-52). *The Examiner is interpreting the buffers of Benveniste which store the uncompressed data to be the caches as instantly claimed.*
- a compressed memory to store a plurality of compressed data; (Column 1 lines 44-47).

- and a compressed memory pointer table (CMPT) to store a plurality of pointers (Column1 line 54 to Column 2 line 11). *The Examiner is interpreting the directory structure of Benveniste to be the pointer table that stores a plurality of pointers pointing to the data as instantly claimed. Each directory entry in the directory structure maintains an address or pointer to the respective data. Accordingly, the directory structure of Benveniste anticipates the pointer table as instantly claimed.*

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache; (Column 1 lines 10-12).

As per dependent claim **27**, Benveniste teach, wherein the compression cache is a sectored cache (Item 266 of Figure 2). *The Examiner notes that as discussed supra, the buffers of Benveniste anticipate the compression cache as instantly claimed. As shown in Figure 2, these buffers are individual and thus sectored. Accordingly Benveniste anticipates the compression cache as a sectored cache with the buffers.*

As per dependent claim **28**, Benveniste teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus (Column1 line 54 to Column 2 line 11). *The Examiner notes that the individual directory entries as a whole anticipate the plurality of tags.*

As per dependent claim **29**, Benveniste teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 1 line 54-60).

Claims 8, 13, and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Benvensite in view of Hasan (U.S. 6,044,416).

As per dependent claim **8**, Benveniste teach, the limitations as noted supra.

Benveniste does not teach, wherein the entry is evicted based on a first in first out (FIFO) protocol.

Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17).

Benveniste and Hasan are analogous art because they are from the same field of endeavor, namely memory configuration.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Hasan before him/her, to combine the FIFO protocol of Hasan into Benveniste for the benefit of a FIFO queue.

The suggestion for doing so is that Hasan shows that when FIFO is used, data that is received from an external input device is stored in sequential order and subsequently provided to the external output device in the same sequential order (Column 1 lines 13-17).

Therefore it would have been obvious to combine the FIFO interface of Hasan with Benveniste for the benefit of a FIFO queue to obtain the invention as specified in claim 8.

As per dependent claim **13**, Benveniste teach, the limitations as noted supra.

Benveniste does not teach, wherein the entry is evicted based on a first in first out (FIFO) protocol.

Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17).

Benveniste and Hasan are analogous art because they are from the same field of endeavor, namely memory configuration.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Hasan before him/her, to combine the FIFO protocol of Hasan into Benveniste for the benefit of a FIFO queue.

The suggestion for doing so is that Hasan shows that when FIFO is used, data that is received from an external input device is stored in sequential order and subsequently provided to the external output device in the same sequential order (Column 1 lines 13-17).

Therefore it would have been obvious to combine the FIFO interface of Hasan with Benveniste for the benefit of a FIFO queue to obtain the invention as specified in claim 13..

As per dependent claim **25**, Benveniste teach, the limitations as noted supra.

Benveniste does not teach, wherein the entry is evicted based on a first in first out (FIFO) protocol.

Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17).

Benveniste and Hasan are analogous art because they are from the same field of endeavor, namely memory configuration.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Hasan before him/her, to combine the FIFO protocol of Hasan into Benveniste for the benefit of a FIFO queue.

The suggestion for doing so is that Hasan shows that when FIFO is used, data that is received from an external input device is stored in sequential order and subsequently provided to the external output device in the same sequential order (Column 1 lines 13-17).

Therefore it would have been obvious to combine the FIFO interface of Hasan with Benveniste for the benefit of a FIFO queue to obtain the invention as specified in claim 25.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. U.S. 3,490,005 Anderson et al teach an instruction handling unit for loops within a program.

2. U.S. 6,101,581 Doren et al teach victim buffers.

3. U.S. 6,173,381 Dye teaches a memory controller using compression and decompression engines.

4. U.S. 6,775,751 Tremaine teaches a system and method for using a compressed main memory.

5. U.S. 6,795,897 Benveniste et al teach a compressed main memory system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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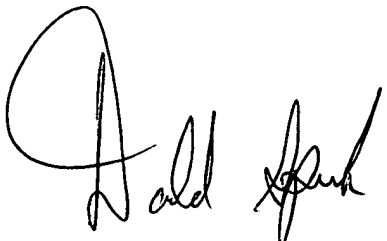

DONALD SPARKS
SUPERVISORY PATENT EXAMINER